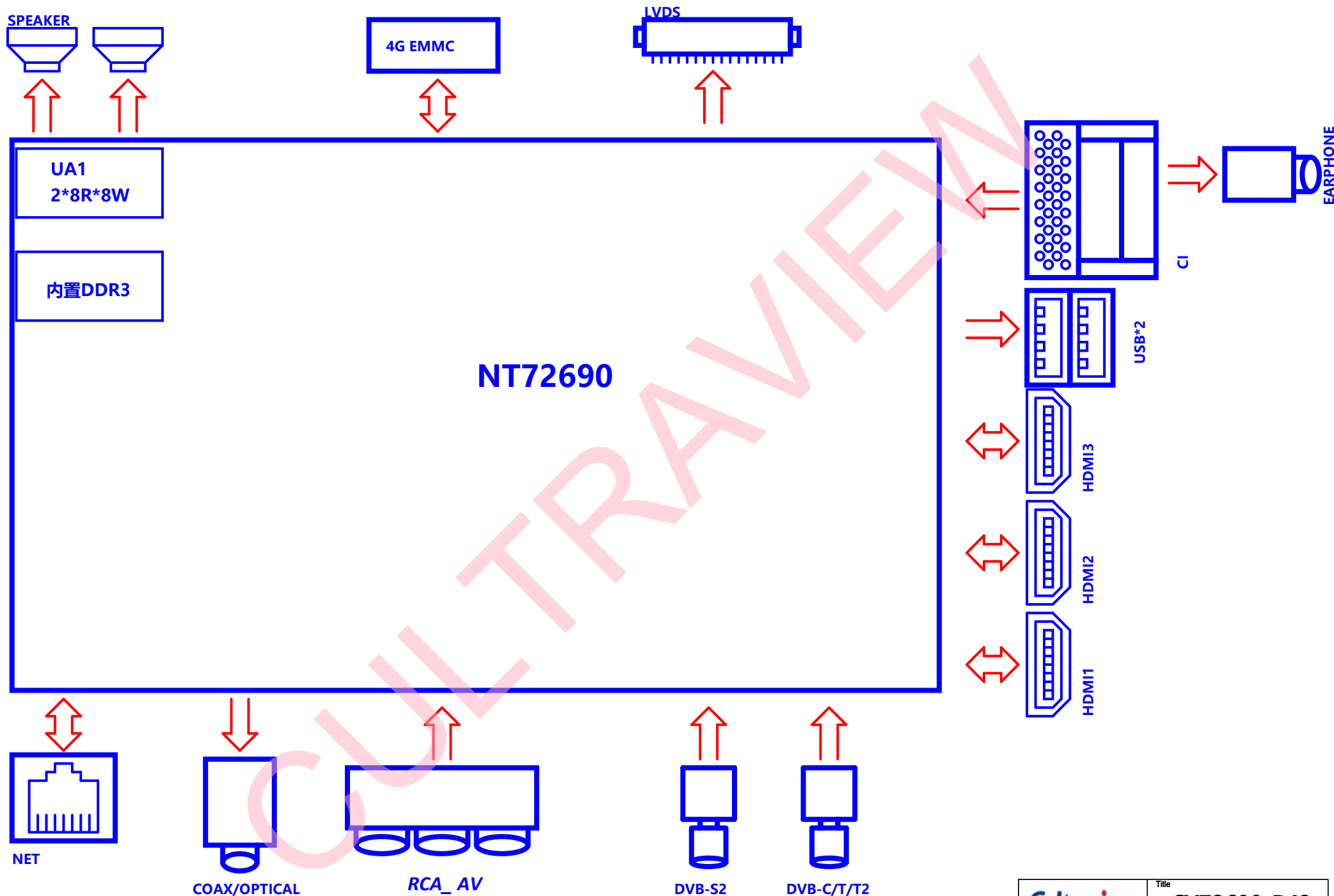
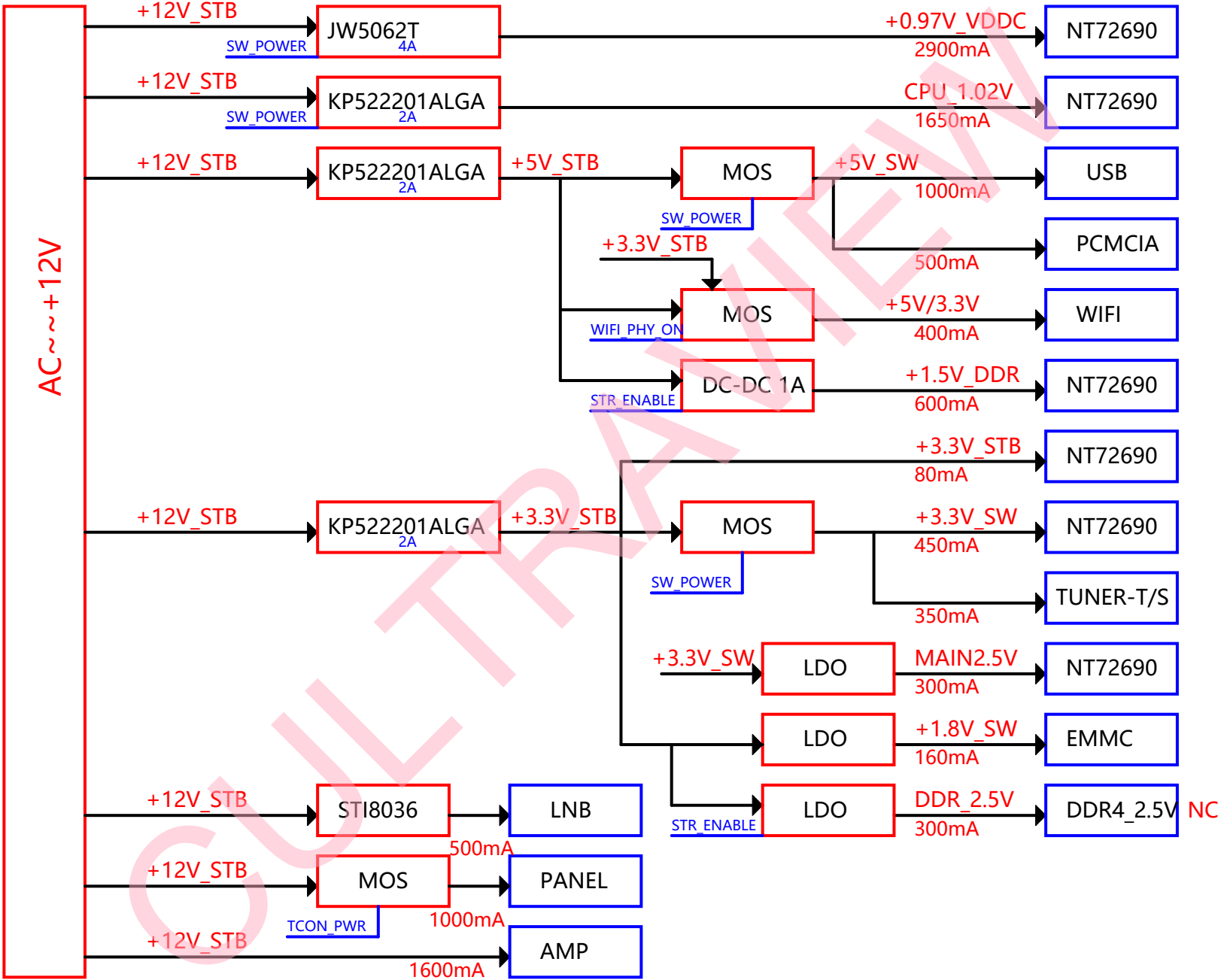
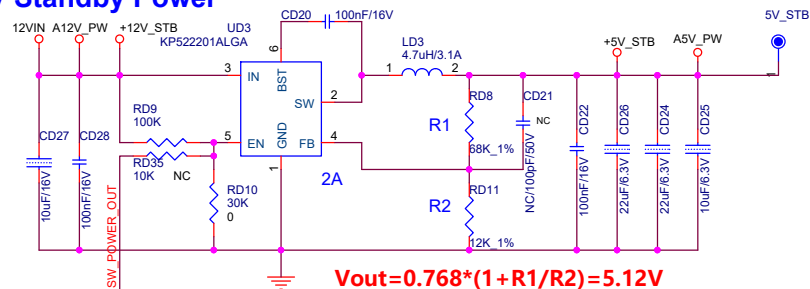




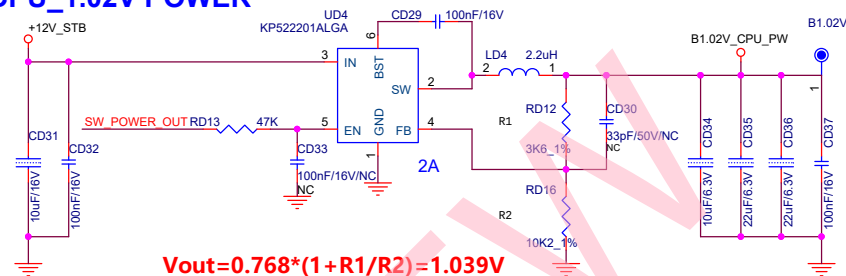
POWER SUPPLY ARCHITECTURE



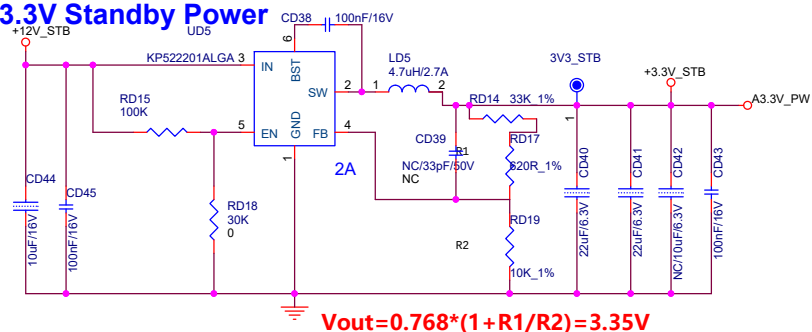
5V Standby Power



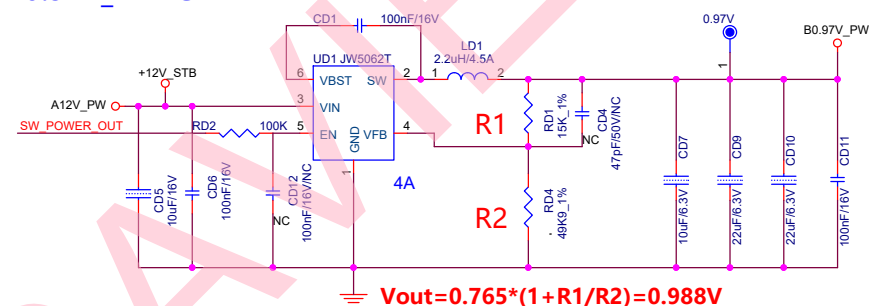
CPU_1.02V POWER



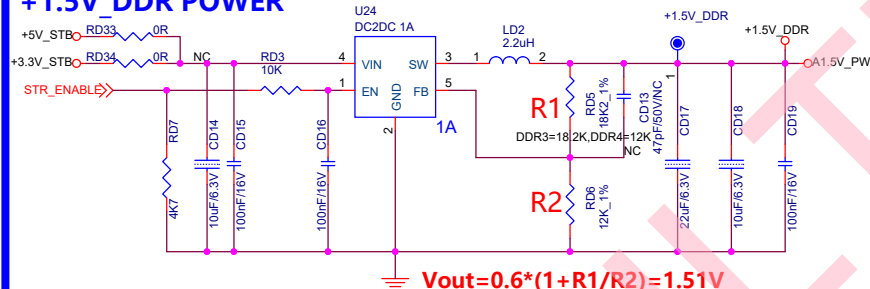
3.3V Standby Power



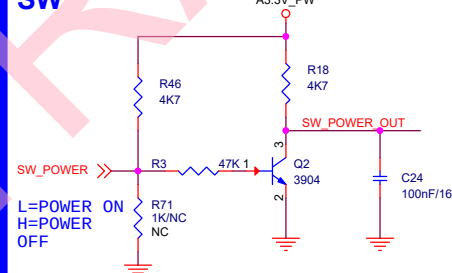
+0.97V_VDDC



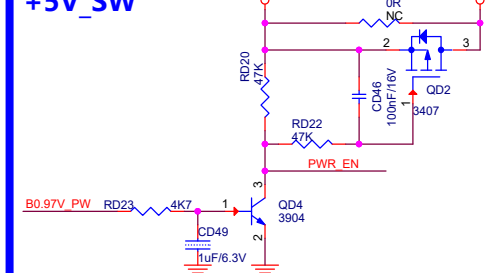
+1.5V_DDR POWER



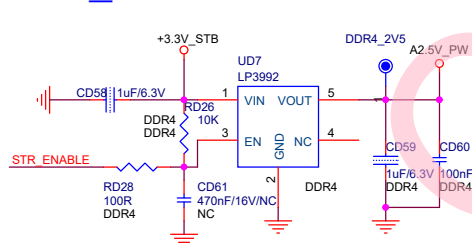
SW



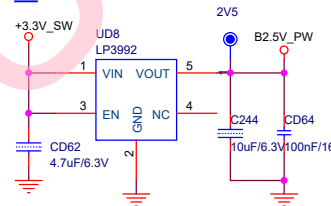
+5V_SW



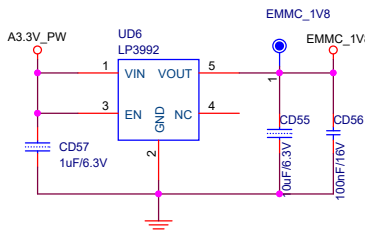
DDR4_2.5V



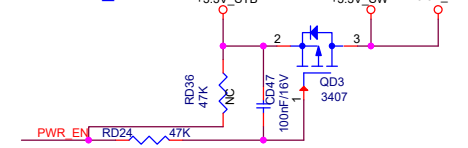
MAIN_2.5V



EMMC 1.8V



+3.3V_SW



Cultraview

Title
CV72690_R42

Size
A3

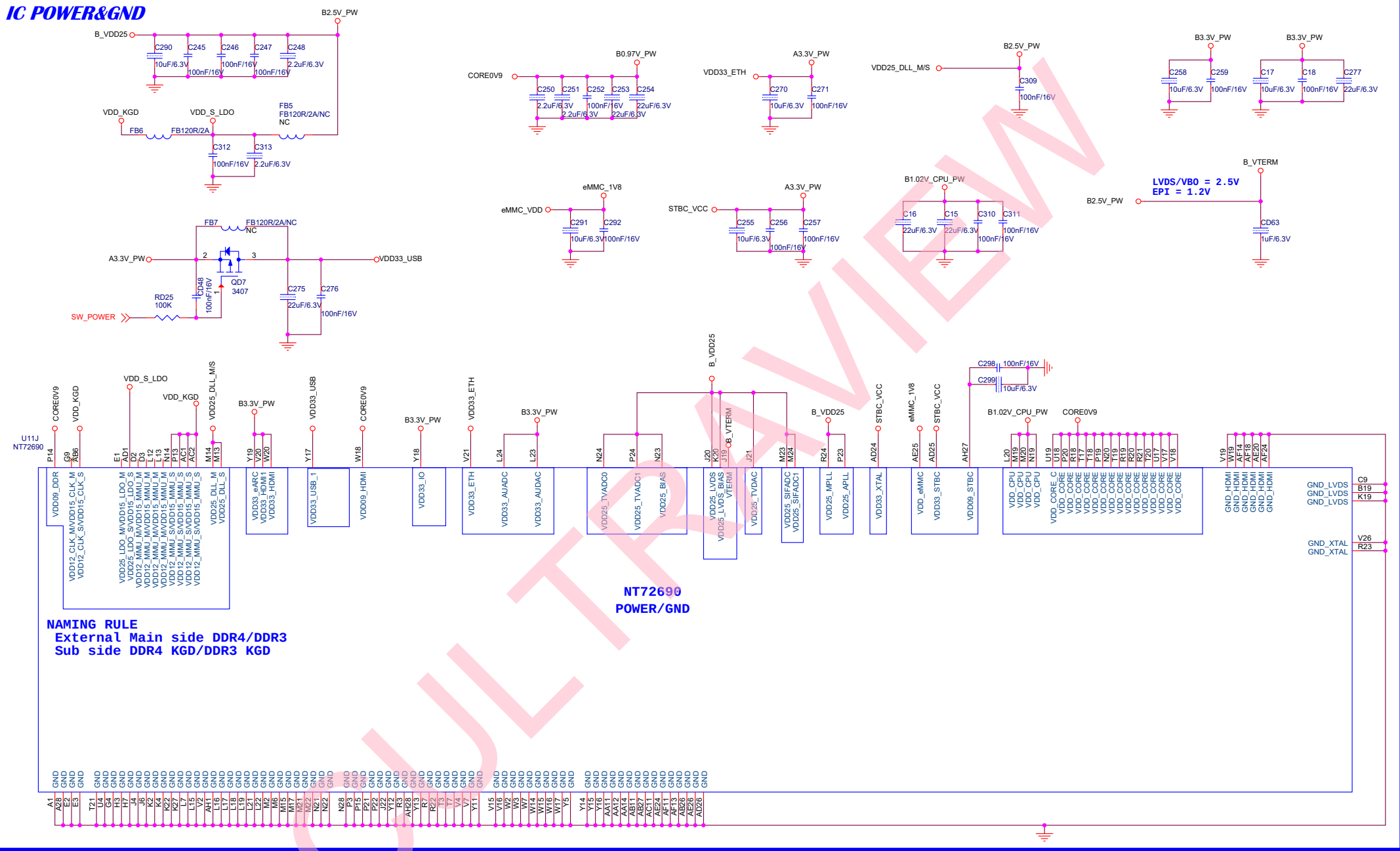
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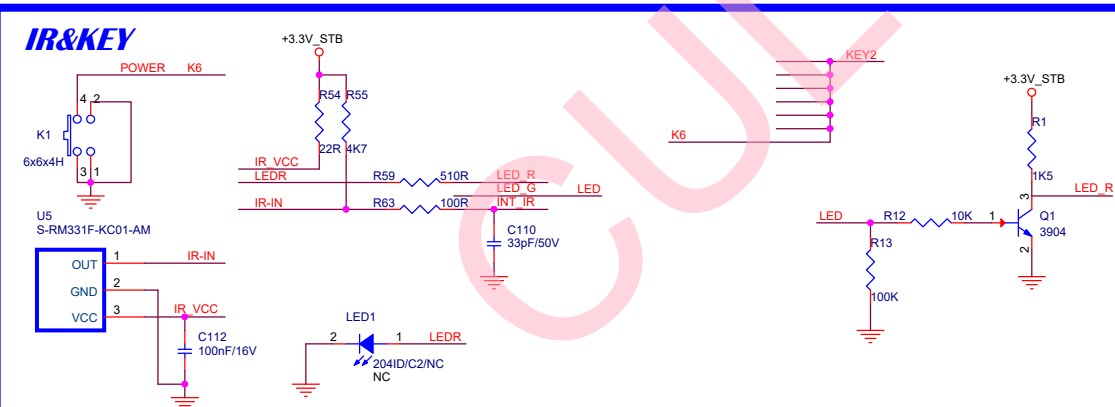
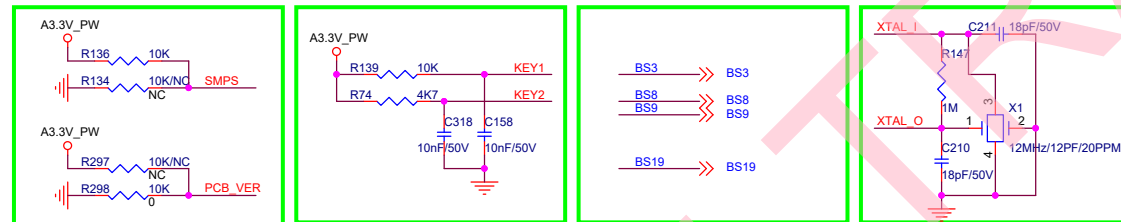
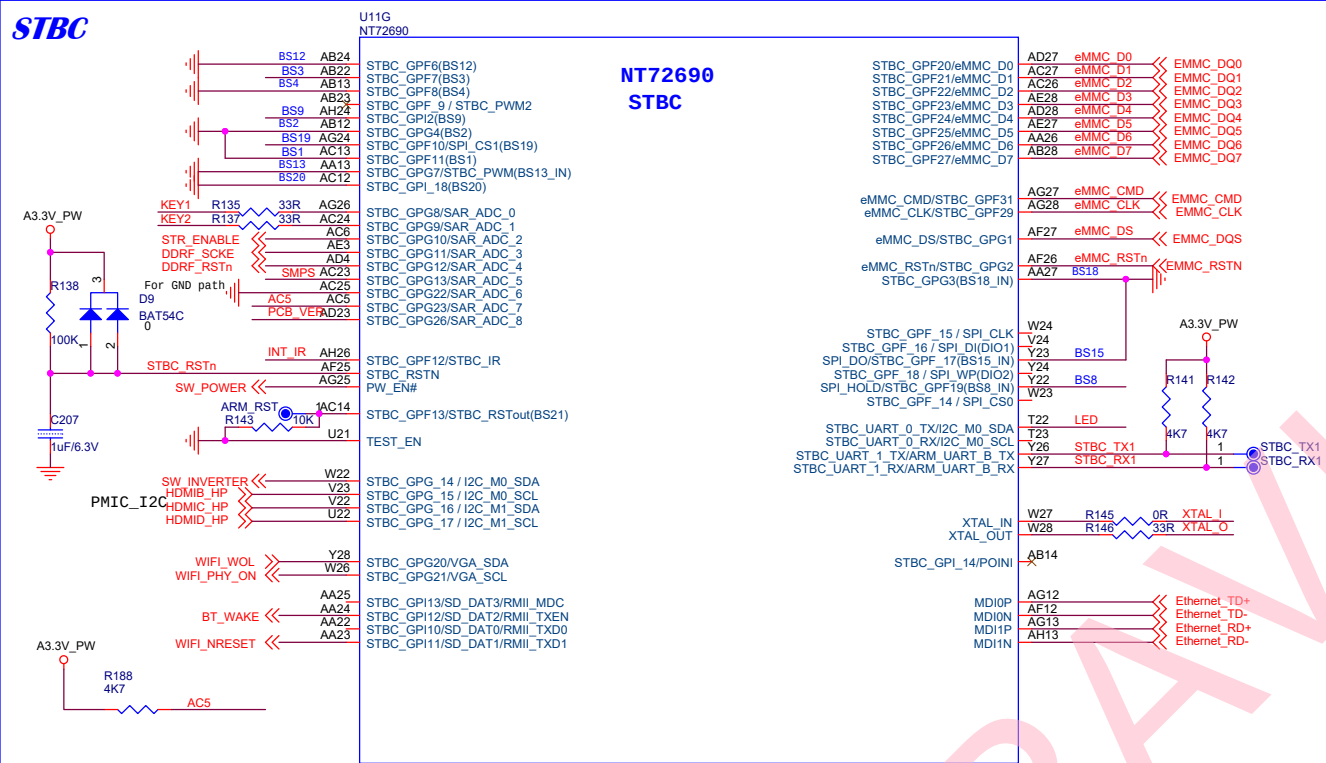
01.POWER

Rev
V10

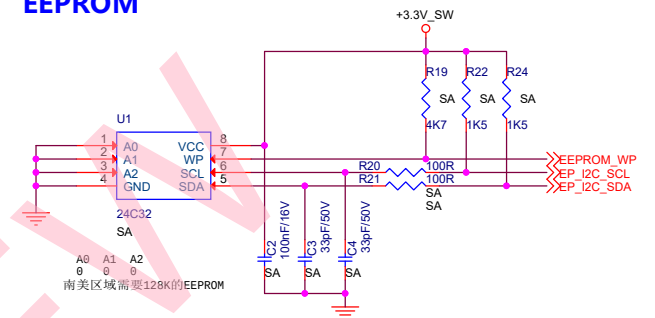
Date: Friday, October 25, 2024

Sheet 2 of 14

IC POWER&GND

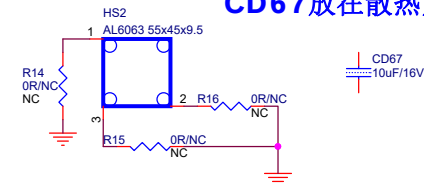
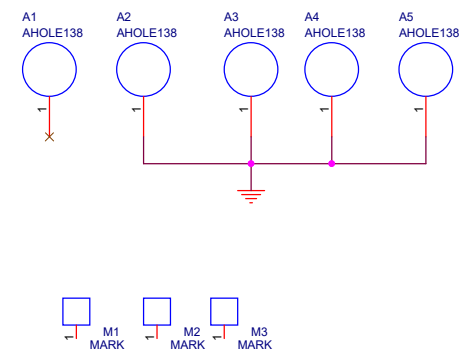
IR&KEY

EEPROM

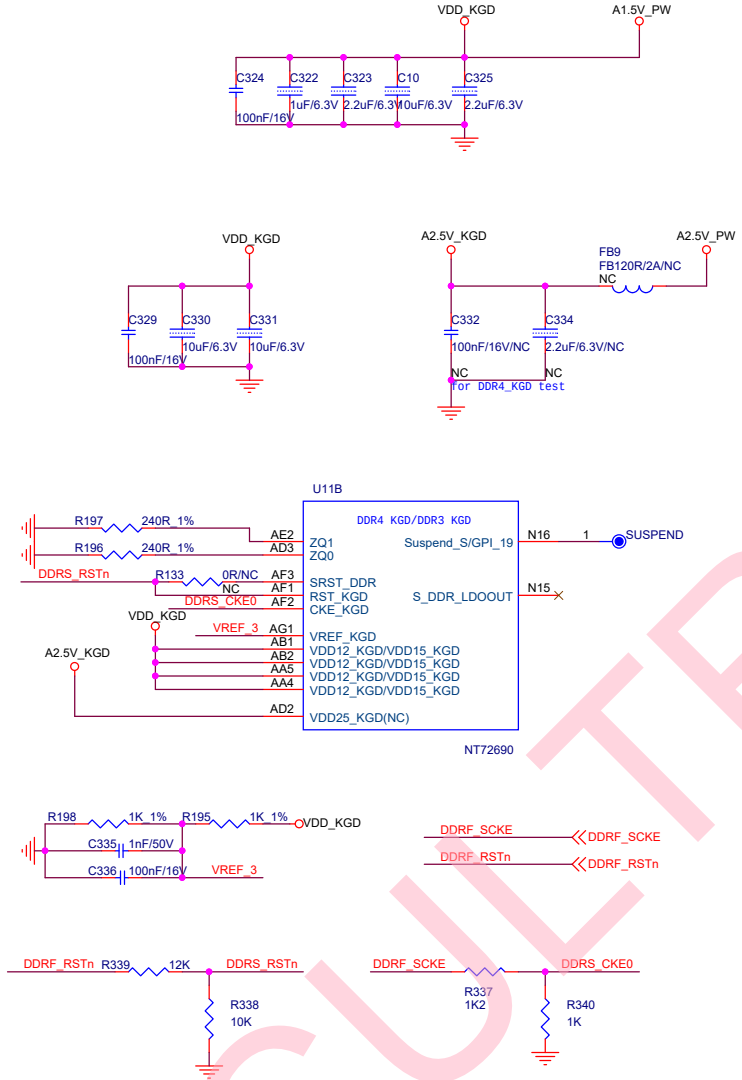


Heat Sink

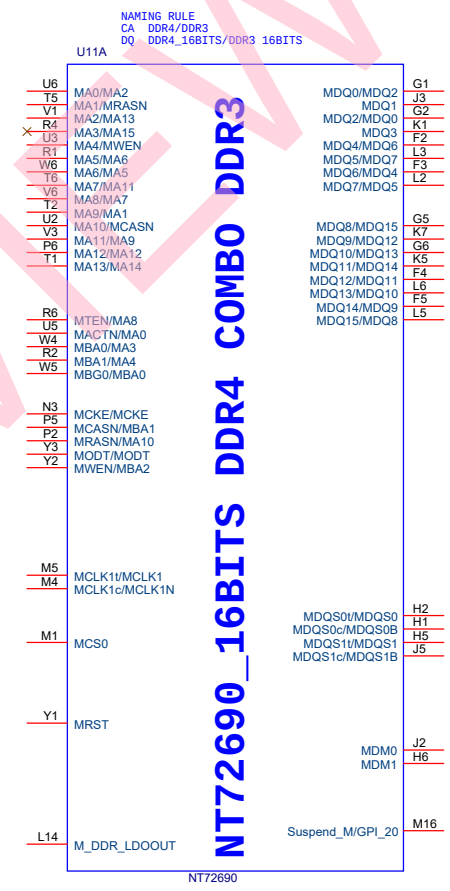
CD67放在散热片右下角做支撑

**MARK & HOLE**

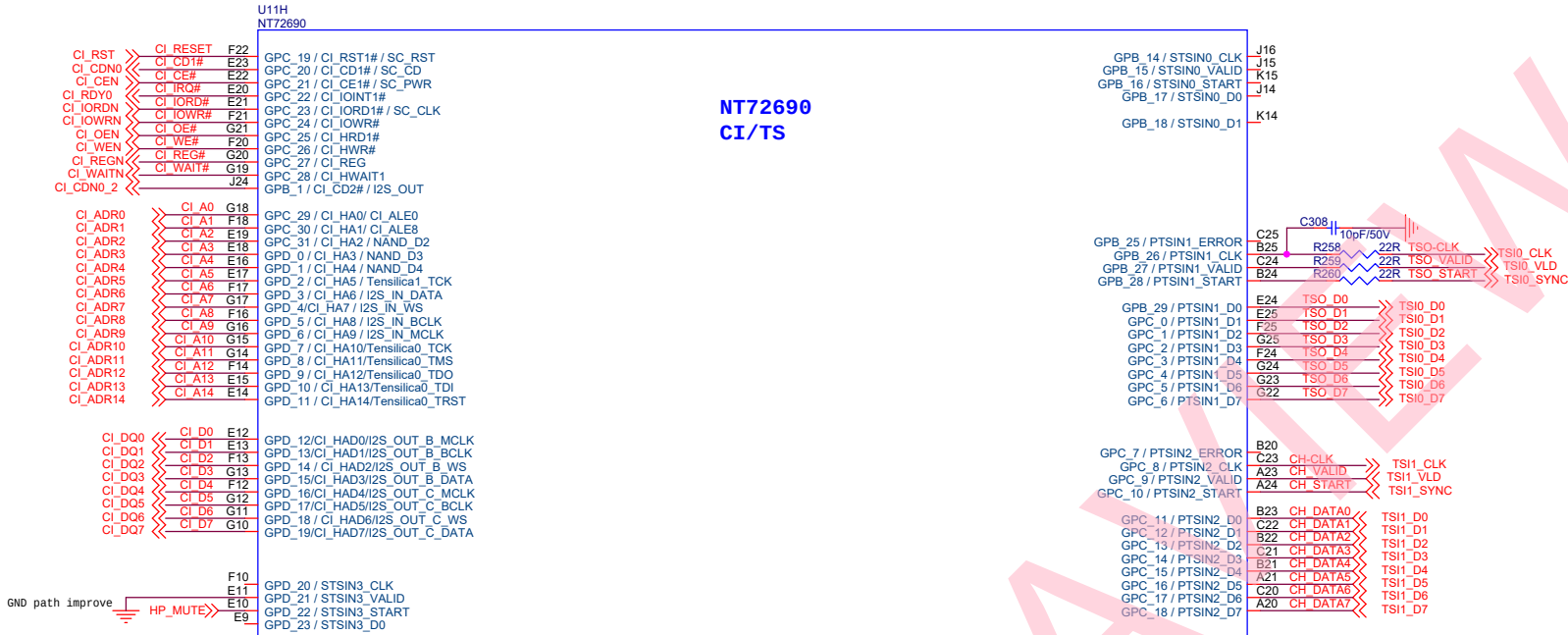
DDR_S



DDR_M



NT72690 CI/TS



CPU Side:

BS0_Bypass CPU MaskROM

0 : Using CPU MaskROM
1 : Bypass CPU MaskROM

STBC Side:

BS1_STBC Boot Strap Option

0: Boot from STBC
1: Boot from CPU, bypass STBC.

BS8_STBC watchdog

0: Default disable STBC watchdog
1: Default enable STBC watchdog

BS19_Internal boot strap for NF/eMMC type

0: NF/eMMC type internal boot strap enable
1: NF/eMMC type internal boot strap disable
(BS[7:6] = 00, BS8 is external; BS[17:16]=00, BS14=0, BS13, BS15, BS18 are external)

BS2_Bypass STBC MaskROM

When BS1=0,
0: Through STBC MaskROM
1: Bypass STBC MaskROM

BS12=0 , BS3,BS4_Device

BS4, 3 =
00: STBC boot from SPI, CPU boot from eMMC
01: STBC & CPU both boot from eMMC
10: STBC & CPU both boot from SPI
11: Reserved (same 00)

eMMC:

BS13_eMMC bus width

BS13 =
0: EMMC Bus width is 8 bit
1: EMMC Bus width is 4 bit

BS15_eMMC ACK

0: Boot mode wait ACK
1: Boot mode do not wait ACK

BS18_eMMC clk_switch

0: 26M
1: 13M

BS9_Security boot

0: no security boot
1: security boot

BS20_NAND I/O

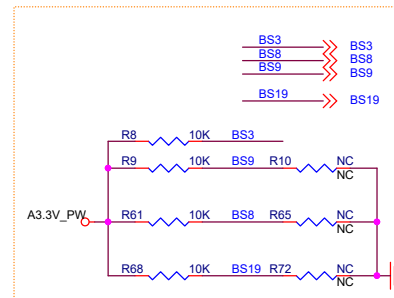
0: NAND I/O in STBC eMMC side (BS12 = 1)
1: NAND I/O in ARM CI side (BS12 = 1, BS[4:3] = 00, 11)
or STBC SPI side (BS12 = 1, BS[4:3] = 01, 10)

BS10_SPI Flash scramble

0: Disable
1: Enable

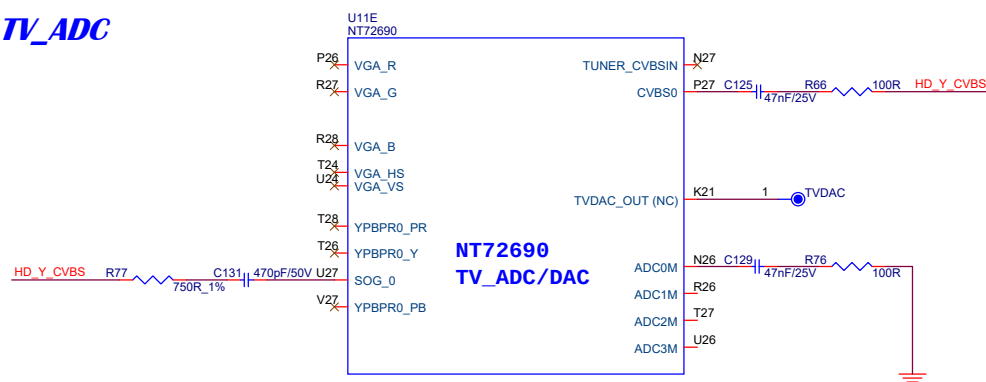
BS11_Turnkey Security

0: Disable
1: Enable

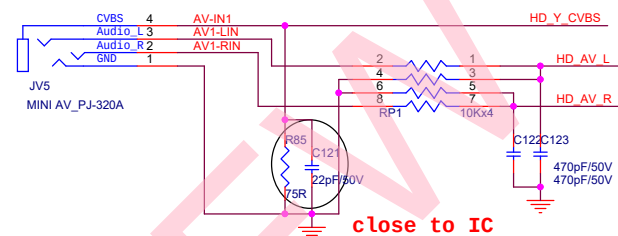
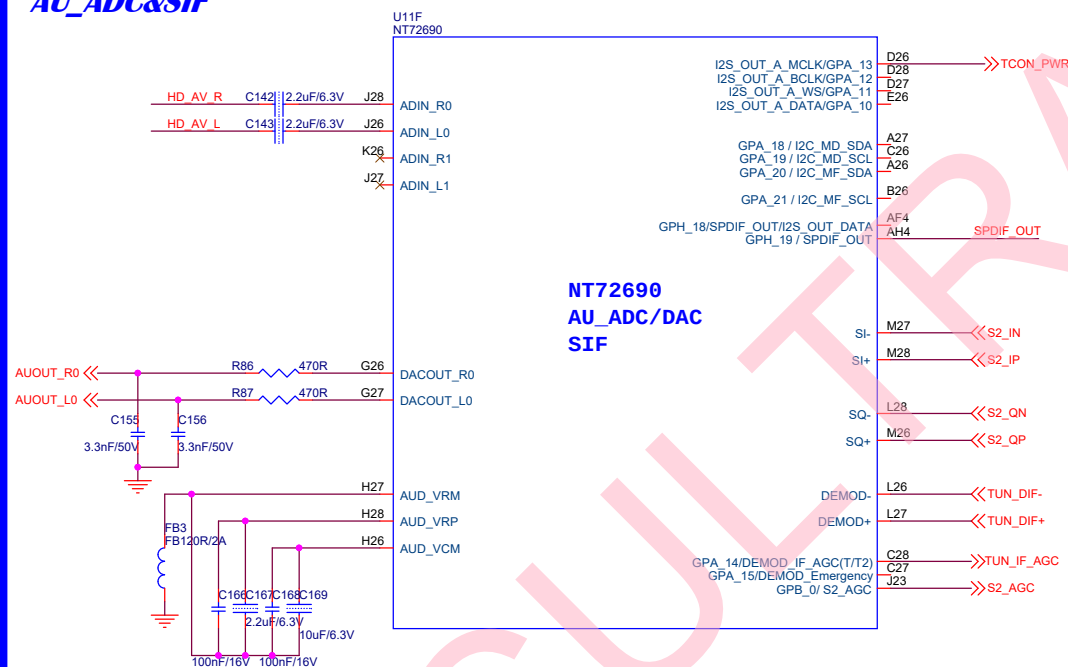


Cultraview

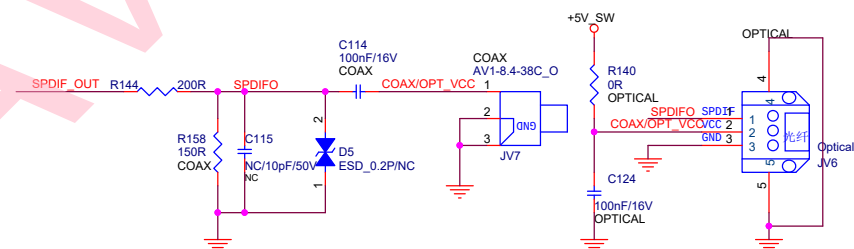
Title
CV72690_R42

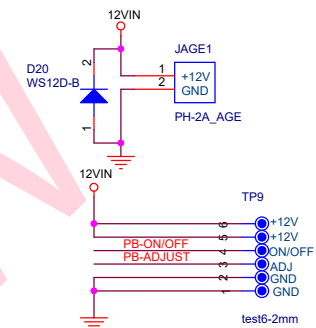
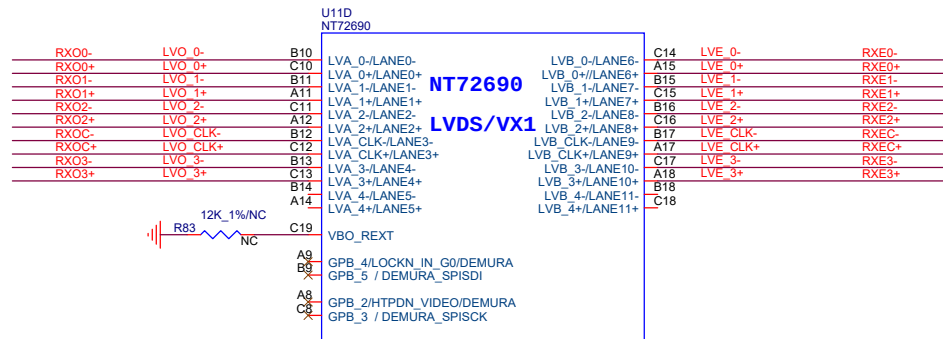
TV_ADC

AV1_IN

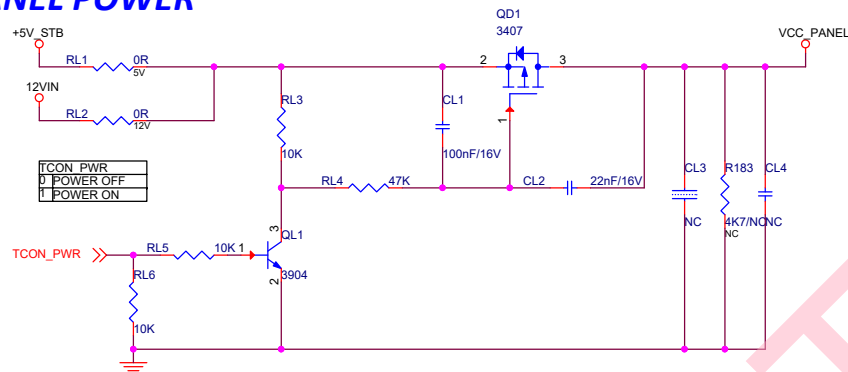
***AU_ADC&SIF***

SPDIF OUT

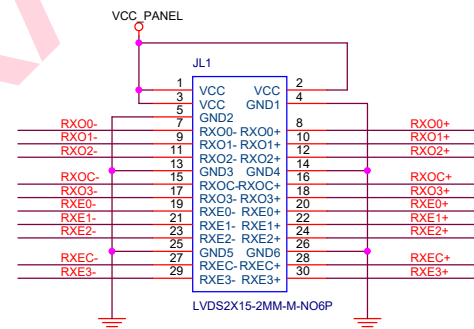




PANEL POWER



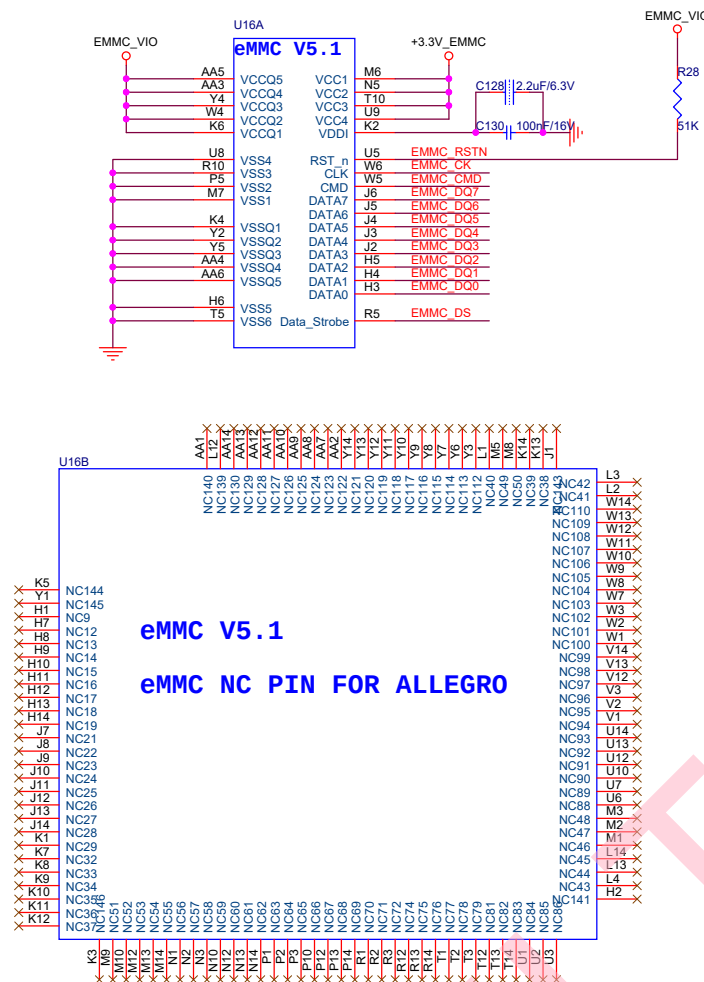
LVDS



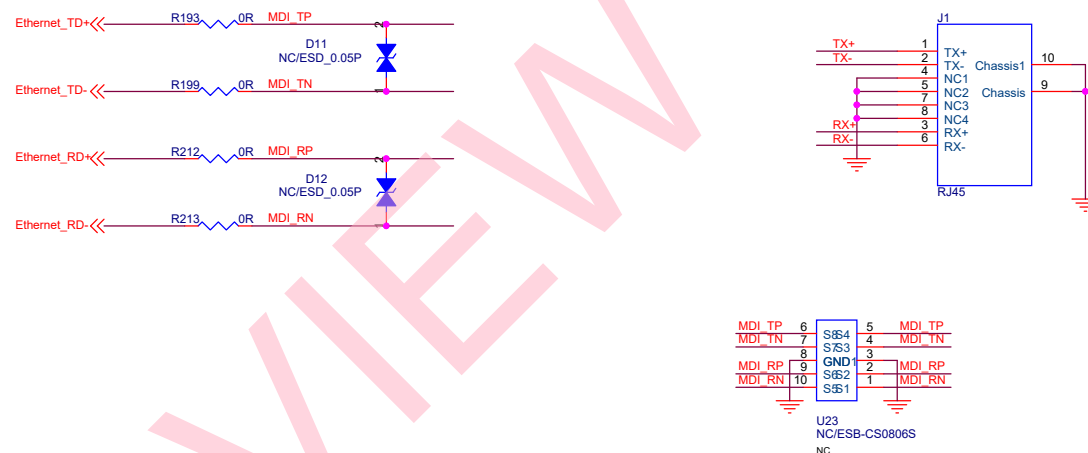
BackLight Controler



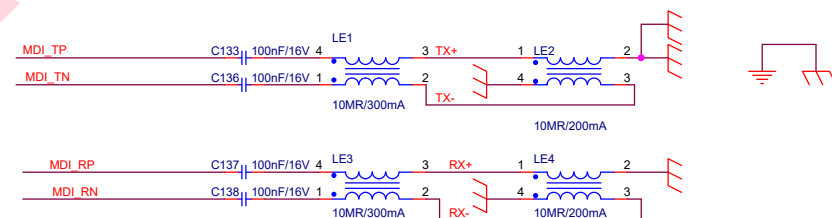
EMMC



Ethernet Connetor



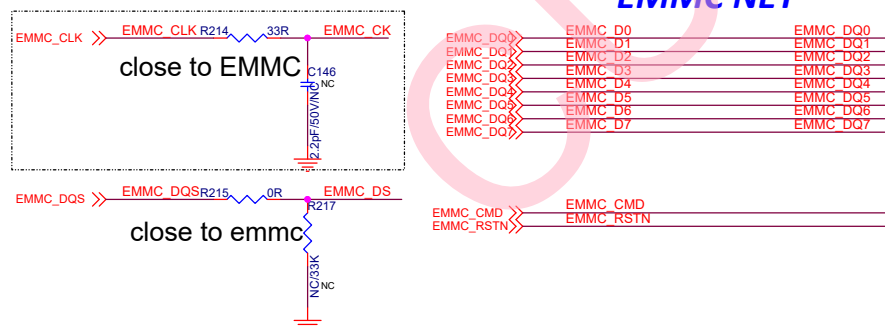
ENTHERNET 分立



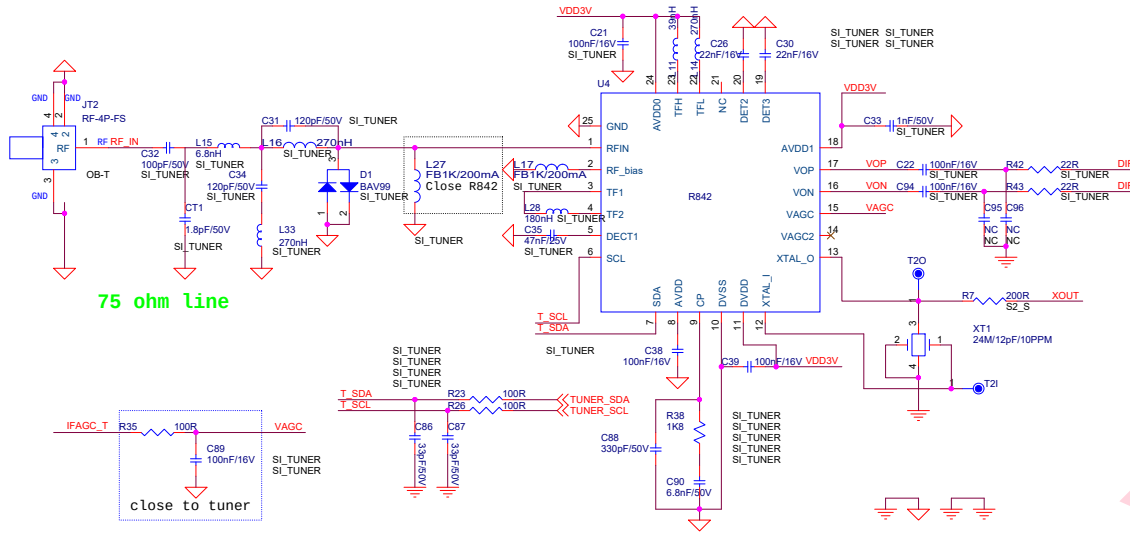
EMMC Power



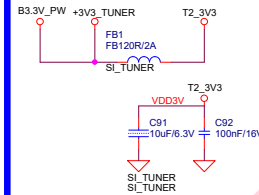
EMMC NET



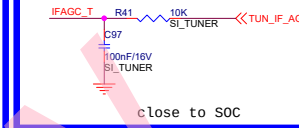
T/T2/C TUNER



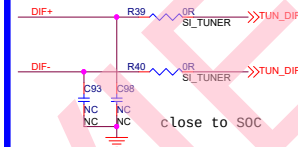
T2 Tuner Power



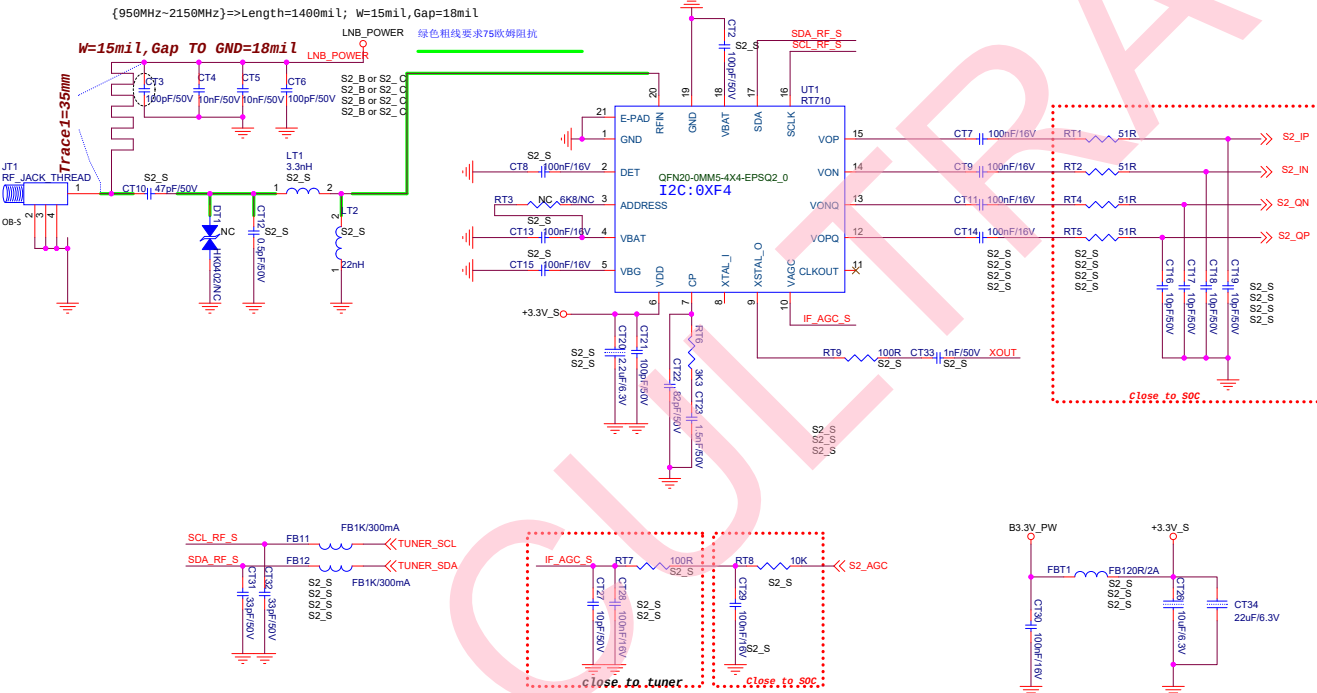
T2_AGC



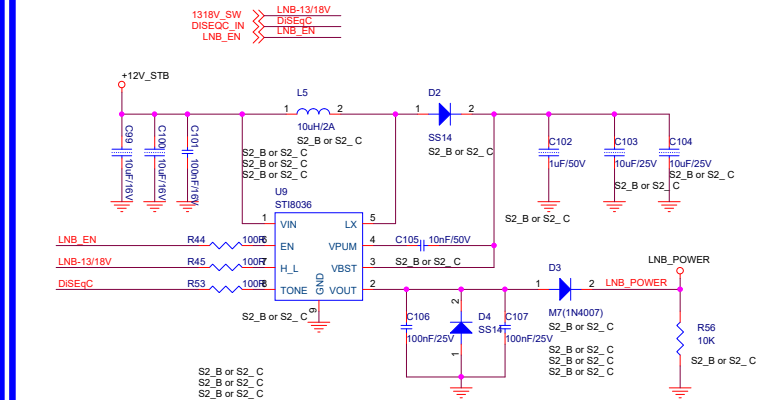
T2_IF



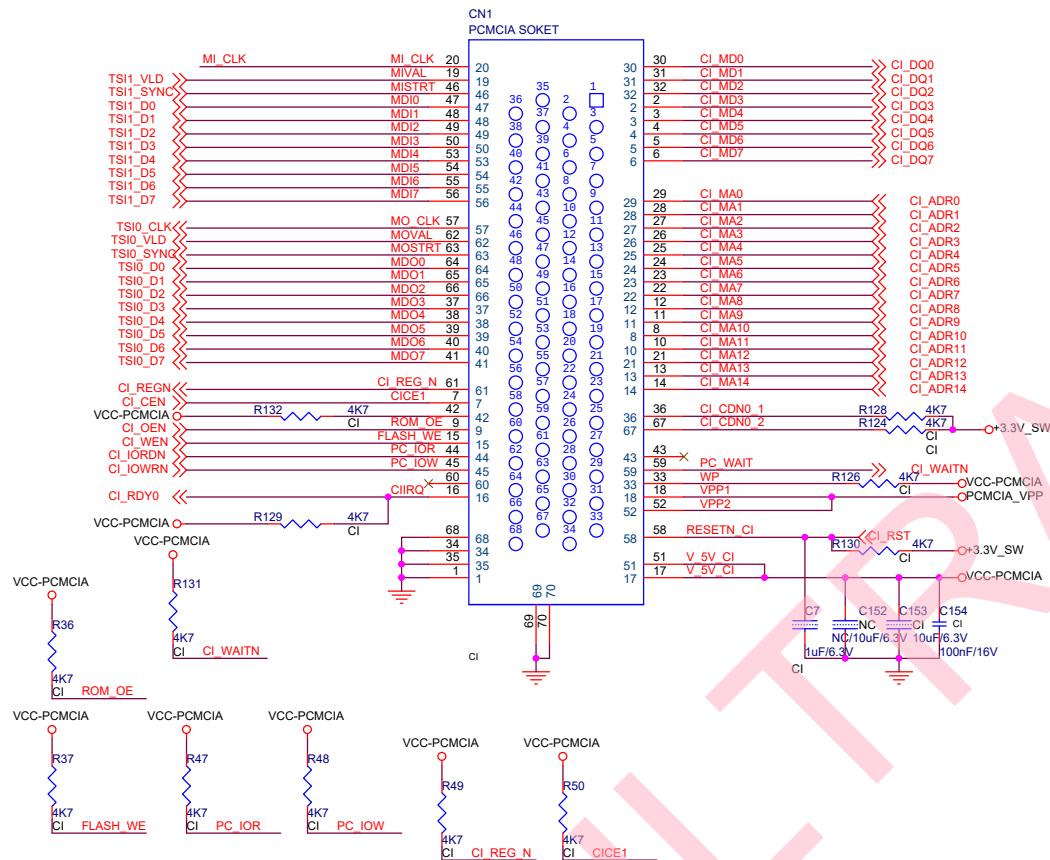
S2 TUNER



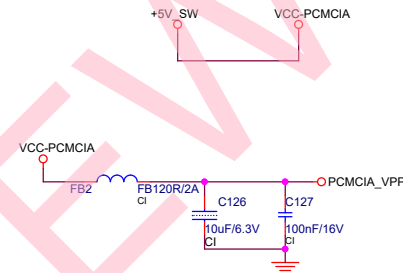
LNB POWER



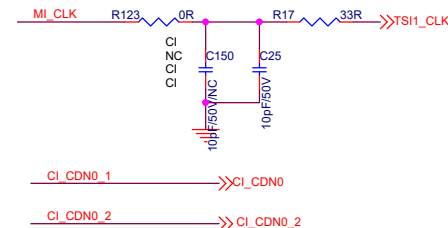
CI Socket



PCMCIA POWER



CLK



AMPLIFY

Diagram illustrating the AMPLIFY circuit, showing the connection of the UA1 HAA3603 op-amp to various input and output pins, including power supply connections (PVCC1, PVCC2, PVCC3), feedback components (FBA1, FBA2, FBA3, FBA4), and output components (CA1, CA2, CA3, CA4, CA5, CA6, CA7, CA8, CA9, CA10, CA11, CA12, CA13, CA14, CA15, CA16, CA17, CA18, CA19, CA20, CA21).

Key components and connections:

- UA1 HAA3603** op-amp.
- Power Supply:** PVCC1, PVCC2, PVCC3.
- Feedback Components:** FBA1, FBA2, FBA3, FBA4.
- Output Components:** CA1, CA2, CA3, CA4, CA5, CA6, CA7, CA8, CA9, CA10, CA11, CA12, CA13, CA14, CA15, CA16, CA17, CA18, CA19, CA20, CA21.
- Resistors:** RA1, RA2, RA3, RA4, RA5.
- Capacitors:** CA1, CA2, CA3, CA4, CA5, CA6, CA7, CA8, CA9, CA10, CA11, CA12, CA13, CA14, CA15, CA16, CA17, CA18, CA19, CA20, CA21.
- Other Components:** ZXT, SHORT, AMP_EN, AMP_POWER, AMP_OUT+, AMP_OUT-, AMP_RIN, AMP_REF, AMP_LIN, AMP_RIN, AMP_OUT+, AMP_OUT-, AMP_RIN, AMP_REF, AMP_LIN.

Connections to the main chip (CLOSE TO MAIN CHIP) include:

- AMP_OUT_L0 >> AMP_LIN
- AMP_OUT_R0 >> AMP_RIN

Connections to the output (AMP_OUT+) include:

- AMP_OUT+ >> AMP_OUT+

Connections to the input (AMP_IN) include:

- AMP_IN >> AMP_IN

Connections to the power supply (AMP_POWER) include:

- AMP_POWER >> AMP_POWER

Connections to the feedback (FBA1, FBA2, FBA3, FBA4) include:

- FBA1 >> FBA1
- FBA2 >> FBA2
- FBA3 >> FBA3
- FBA4 >> FBA4

Connections to the output (CA1, CA2, CA3, CA4, CA5, CA6, CA7, CA8, CA9, CA10, CA11, CA12, CA13, CA14, CA15, CA16, CA17, CA18, CA19, CA20, CA21) include:

- CA1 >> CA1
- CA2 >> CA2
- CA3 >> CA3
- CA4 >> CA4
- CA5 >> CA5
- CA6 >> CA6
- CA7 >> CA7
- CA8 >> CA8
- CA9 >> CA9
- CA10 >> CA10
- CA11 >> CA11
- CA12 >> CA12
- CA13 >> CA13
- CA14 >> CA14
- CA15 >> CA15
- CA16 >> CA16
- CA17 >> CA17
- CA18 >> CA18
- CA19 >> CA19
- CA20 >> CA20
- CA21 >> CA21

Connections to the input (AMP_IN) include:

- AMP_IN >> AMP_IN

Connections to the power supply (AMP_POWER) include:

- AMP_POWER >> AMP_POWER

Connections to the feedback (FBA1, FBA2, FBA3, FBA4) include:

- FBA1 >> FBA1
- FBA2 >> FBA2
- FBA3 >> FBA3
- FBA4 >> FBA4

Connections to the output (CA1, CA2, CA3, CA4, CA5, CA6, CA7, CA8, CA9, CA10, CA11, CA12, CA13, CA14, CA15, CA16, CA17, CA18, CA19, CA20, CA21) include:

- CA1 >> CA1
- CA2 >> CA2
- CA3 >> CA3
- CA4 >> CA4
- CA5 >> CA5
- CA6 >> CA6
- CA7 >> CA7
- CA8 >> CA8
- CA9 >> CA9
- CA10 >> CA10
- CA11 >> CA11
- CA12 >> CA12
- CA13 >> CA13
- CA14 >> CA14
- CA15 >> CA15
- CA16 >> CA16
- CA17 >> CA17
- CA18 >> CA18
- CA19 >> CA19
- CA20 >> CA20
- CA21 >> CA21

Connections to the input (AMP_IN) include:

- AMP_IN >> AMP_IN

Connections to the power supply (AMP_POWER) include:

- AMP_POWER >> AMP_POWER

Connections to the feedback (FBA1, FBA2, FBA3, FBA4) include:

- FBA1 >> FBA1
- FBA2 >> FBA2
- FBA3 >> FBA3
- FBA4 >> FBA4

Connections to the output (CA1, CA2, CA3, CA4, CA5, CA6, CA7, CA8, CA9, CA10, CA11, CA12, CA13, CA14, CA15, CA16, CA17, CA18, CA19, CA20, CA21) include:

- CA1 >> CA1
- CA2 >> CA2
- CA3 >> CA3
- CA4 >> CA4
- CA5 >> CA5
- CA6 >> CA6
- CA7 >> CA7
- CA8 >> CA8
- CA9 >> CA9
- CA10 >> CA10
- CA11 >> CA11
- CA12 >> CA12
- CA13 >> CA13
- CA14 >> CA14
- CA15 >> CA15
- CA16 >> CA16
- CA17 >> CA17
- CA18 >> CA18
- CA19 >> CA19
- CA20 >> CA20
- CA21 >> CA21

Connections to the input (AMP_IN) include:

- AMP_IN >> AMP_IN

Connections to the power supply (AMP_POWER) include:

- AMP_POWER >> AMP_POWER

Connections to the feedback (FBA1, FBA2, FBA3, FBA4) include:

- FBA1 >> FBA1
- FBA2 >> FBA2
- FBA3 >> FBA3
- FBA4 >> FBA4

Connections to the output (CA1, CA2, CA3, CA4, CA5, CA6, CA7, CA8, CA9, CA10, CA11, CA12, CA13, CA14, CA15, CA16, CA17, CA18, CA19, CA20, CA21) include:

- CA1 >> CA1
- CA2 >> CA2
- CA3 >> CA3
- CA4 >> CA4
- CA5 >> CA5
- CA6 >> CA6
- CA7 >> CA7
- CA8 >> CA8
- CA9 >> CA9
- CA10 >> CA10
- CA11 >> CA11
- CA12 >> CA12
- CA13 >> CA13
- CA14 >> CA14
- CA15 >> CA15
- CA16 >> CA16
- CA17 >> CA17
- CA18 >> CA18
- CA19 >> CA19
- CA20 >> CA20
- CA21 >> CA21

Connections to the input (AMP_IN) include:

- AMP_IN >> AMP_IN

Connections to the power supply (AMP_POWER) include:

- AMP_POWER >> AMP_POWER

Connections to the feedback (FBA1, FBA2, FBA3, FBA4) include:

- FBA1 >> FBA1
- FBA2 >> FBA2
- FBA3 >> FBA3
- FBA4 >> FBA4

Connections to the output (CA1, CA2, CA3, CA4, CA5, CA6, CA7, CA8, CA9, CA10, CA11, CA12, CA13, CA14, CA15, CA16, CA17, CA18, CA19, CA20, CA21) include:

- CA1 >> CA1
- CA2 >> CA2
- CA3 >> CA3
- CA4 >> CA4
- CA5 >> CA5
- CA6 >> CA6
- CA7 >> CA7
- CA8 >> CA8
- CA9 >> CA9
- CA10 >> CA10
- CA11 >> CA11
- CA12 >> CA12
- CA13 >> CA13
- CA14 >> CA14
- CA15 >> CA15
- CA16 >> CA16
- CA17 >> CA17
- CA18 >> CA18
- CA19 >> CA19
- CA20 >> CA20
- CA21 >> CA21

Connections to the input (AMP_IN) include:

- AMP_IN >> AMP_IN

Connections to the power supply (AMP_POWER) include:

- AMP_POWER >> AMP_POWER

Connections to the feedback (FBA1, FBA2, FBA3, FBA4) include:

- FBA1 >> FBA1
- FBA2 >> FBA2
- FBA3 >> FBA3
- FBA4 >> FBA4

Connections to the output (CA1, CA2, CA3, CA4, CA5, CA6, CA7, CA8, CA9, CA10, CA11, CA12, CA13, CA14, CA15, CA16, CA17, CA18, CA19, CA20, CA21) include:

- CA1 >> CA1
- CA2 >> CA2
- CA3 >> CA3
- CA4 >> CA4
- CA5 >> CA5
- CA6 >> CA6
- CA7 >> CA7
- CA8 >> CA8
- CA9 >> CA9
- CA10 >> CA10
- CA11 >> CA11
- CA12 >> CA12
- CA13 >> CA13
- CA14 >> CA14
<

POWER

The diagram shows a power supply circuit. A red wire labeled `+12V_STB` connects to a node labeled `PVDVDD`. From `PVDVDD`, a red wire goes to `AMP_POWER`. A blue capacitor labeled `CA24 470uF/16V` is connected between `PVDVDD` and `GND`. The capacitor has a '+' sign on its top plate.

MUTE

AMP_MUTE

AMP MUTE
0. MUTE
1. NORMAL

RA10 4K7 AMP-EN

RA11 4K7

```
graph TD
    AMP_MUTE[AMP_MUTE] --- RA10[RA10 4K7] --- AMP_EN[AMP-EN]
    AMP_MUTE --- RA11[RA11 4K7] --- GND[Ground]
```

EARPHONE

The diagram shows a circuit for detecting earphone insertion and removal. It features a 3.3V SW supply connected to a network of resistors (RA23, R11, RA26) and a transistor (Q13). The circuit is connected to a jack (JA2) with pins for GND, OUTR, NC, and OUTL. The output of the circuit is IDENT_HP, which is connected to a resistor (R84) and the NC pin of the jack. The circuit also includes capacitors CA37, CA38, CA39, and CA40 for timing and filtering.

JA2

1 2 3 4 5

GND

OUTR

NC

OUTL

PJ-328A

EAR ROUT

EAR DET

EAR LOUT

CA37 100nF/6.3V

CA38 22nF/16V

CA39 100uF/6.3V

CA40 22nF/16V

+3.3V_SW

RA23 47K

R11 4K7

RA26 4K7

Q13 3904

R84 4K7/NC NC

IDENT_HP

Earphone Detect
H: Insert Earphone;
L: Pull Out Earphone;

